What is claimed is:

1. A multiplier for multiplying a first signal and a second signal, the first signal representing a first binary number $a = [a_{N-1} \ldots a_1 a_0]$, the second signal representing a second binary number $b = [b_{N-1} \ldots b_1 b_0]$, the multiplier comprising:

a first port for receiving the first signal;

a second port for receiving the second signal;

a triangle array operatively coupled to the first signal and the second signal; and

an adder for adding elements of the triangle array to produce a third signal representing a product of the first signal and the second signal.

2. The multiplier according to claim 1, wherein the triangle array includes lines $k = 0$ to N-1, such that:

the line $k = 0$ of the triangle array is equal to $[0\ (a_0 * b_0)]$; and

the lines $k = 1$ to N-1 of the triangle array are equal to $[p_1\ p0\ d_{k-1} \ldots d_1\ d_0]$, wherein the peak bits $[p_1\ p0]$ for each line k are determined by:

$[p_1\ p0] = [0\ 0]$ if $a_k * b_k \neq 1$,

$[p1\ p0] = [1\ 0]$ if $[a_k * b_k = 1$ AND $c_k = 1]$, and

$[p1\ p0] = [0\ 1]$ if $[a_k * b_k = 1$ AND $c_k = 0]$,

wherein $[d_{k-1} \ldots d_1\ d_0]$ for each line k are determined by:

$[d_{k-1} \ldots d_1\ d_0] = [0_{k-1} \ldots 0_0]$ if $[a_k\ b_k] = [0\ 0]$,

$[d_{k-1} \ldots d_1\ d_0] = [a_{k-1} \ldots a_1\ a_0]$ if $[a_k\ b_k] = [0\ 1]$,

$[d_{k-1} \ldots d_1\ d_0] = [b_{k-1} \ldots b_1\ b_0]$ if $[a_k\ b_k] = [1\ 0]$, and

$[d_{k-1} \ldots d_1\ d_0] = [s_{k-1} \ldots s_1\ s_0]$ if $[a_k\ b_k] = [1\ 1]$,

and wherein $s = [s_{N-2} \ldots s_1\ s_0]$ is equal to the sum sequence $[(a_{N-2} + b_{N-2}) \ldots (a_1+b_1)\ (a_0+b_0)]$ and $c = [c_{N-1} \ldots c_1]$ is equal to the carry sequence associated with the sum sequence s.

3. The multiplier according to claim 2, further comprising a second adder for producing the sum sequence s and the carry sequence c.

4. The multiplier according to claim 2, further comprising at least one multiplexer for producing $[d_{k-1} \ldots d_1\ d_0]$ for each line k.

5. The multiplier according to claim 4, wherein the multiplexer is a four to one multiplexer having as inputs 0, the first signal, the second signal, and the sum sequence s, the multiplexer controlled by $[a_k\ b_k]$.

6. The multiplier according to claim 1, wherein the triangle array is represented by a number of digits that is substantially 30% less than the number of digits required in a diamond array.

7. The multiplier according to claim 1, wherein the triangle array is represented by a number of digits that is substantially 50% less than the number of digits required in a diamond array.

8. A processor for multiplying a first signal and a second signal, the first signal representing a first binary number $a = [a_{N-1} \ldots a_1\ a_0]$, the second signal representing a second binary number $b = [b_{N-1} \ldots b_1\ b_0]$, the processor comprising:

input means for receiving the first signal and the second signal;

means for forming a triangle array as a function of the first signal and the second signal; and

an adder for adding elements of the triangle array to form a third signal representing a product of the first signal and the second signal.

9. The processor according to claim 8, wherein the triangle array includes lines $k = [0\ 1 \ldots N\text{-}1]$, such that:

the line $k = 0$ of the triangle array is equal to $[0\ (a_0 * b_0)]$; and

the lines $k = 1$ to N-1 of the triangle array are equal to $[p_1\ p0\ d_{k-1} \ldots d_1\ d_0]$,

wherein the peak bits $[p_1\ p0]$ for each line k are determined by:

$[p_1\ p0] = [0\ 0]$ if $a_k * b_k \neq 1$,

$[p1\ p0] = [1\ 0]$ if $[a_k * b_k = 1$ AND $c_k = 1]$, and

$[p1\ p0] = [0\ 1]$ if $[a_k * b_k = 1$ AND $c_k = 0]$,

wherein $[d_{k-1} \ldots d_1\ d_0]$ for each line k are determined by:

$[d_{k-1} \ldots d_1\ d_0] = [0_{k-1} \ldots 0_0]$ if $[a_k\ b_k] = [0\ 0]$,

$[d_{k-1} \ldots d_1\ d_0] = [a_{k-1} \ldots a_1\ a_0]$ if $[a_k\ b_k] = [0\ 1]$,

$[d_{k-1} \ldots d_1\ d_0] = [b_{k-1} \ldots b_1\ b_0]$ if $[a_k\ b_k] = [1\ 0]$, and

$[d_{k-1} \ldots d_1\ d_0] = [s_{k-1} \ldots s_1\ s_0]$ if $[a_k\ b_k] = [1\ 1]$,

and wherein $s = [s_{N-2} \ldots s_1 s_0]$ equal to the sum sequence $[(a_{N-2} + b_{N-2}) \ldots (a_1+b_1) (a_0+b_0)]$ and $c = [c_{N-1} \ldots c_1]$ is equal to the carry sequence associated with the sum sequence s.

10. The processor according to claim 9, wherein the means for forming the triangle array include a second adder for producing the sum sequence s and the carry sequence c.

11. The processor according to claim 9, wherein the means for forming the triangle array includes at least one multiplexer for producing $[d_{k-1} \ldots d_1 d_0]$ for each line k.

12. The processor according to claim 11, wherein the multiplexer is a four to one multiplexer having as inputs 0, the first signal, the second signal, and the sum sequence s, the multiplexer controlled by $[a_k b_k]$.

13. The processor according to claim 8, wherein the triangle array is represented by a number of digits that is substantially 30% less than the number of digits required in a diamond array.

14. The processor according to claim 8, wherein the triangle array is represented by a number of digits that is substantially 50% less than the number of digits required in a diamond array.

15. A computer program product for use on a computer system for multiplying a first binary number $a = [a_{N-1} \ldots a_1 a_0]$ and a second binary number $b = [b_{N-1} \ldots b_1 b_0]$, the computer program product comprising a computer usable medium having computer readable program code thereon, the computer readable program code comprising:

program code for forming a triangle array from the first binary number and the second binary number, the triangle array including lines k = 0 to N-1; and

program code for adding lines k = 0 to N-1.

16. The computer program product according to claim 15, wherein the program code for forming the triangle array includes:

program code for producing line k = 0, wherein line k=0 is equal to $[0\ (a_0 * b_0)]$;

program code for producing lines $k = 1$ to N-1 of the triangle array, wherein lines $k=1$ to N-1 are equal to $[p_1\ p0\ d_{k-1} \ldots d_1\ d_0]$, wherein the peak bits $[p_1\ p0]$ for each line k are determined by:

$[p_1\ p0] = [0\ 0]$ if $a_k * b_k \neq 1$,

$[p1\ p0] = [1\ 0]$ if $[a_k * b_k = 1$ AND $c_k = 1]$, and

$[p1\ p0] = [0\ 1]$ if $[a_k * b_k = 1$ AND $c_k = 0]$,

wherein $[d_{k-1} \ldots d_1\ d_0]$ for each line k are determined by:

$[d_{k-1} \ldots d_1\ d_0] = [0_{k-1} \ldots 0_0]$ if $[a_k\ b_k] = [0\ 0]$,

$[d_{k-1} \ldots d_1\ d_0] = [a_{k-1} \ldots a_1\ a_0]$ if $[a_k\ b_k] = [0\ 1]$,

$[d_{k-1} \ldots d_1\ d_0] = [b_{k-1} \ldots b_1\ b_0]$ if $[a_k\ b_k] = [1\ 0]$, and

$[d_{k-1} \ldots d_1\ d_0] = [s_{k-1} \ldots s_1\ s_0]$ if $[a_k\ b_k] = [1\ 1]$,

and wherein $s = [s_{N-2} \ldots s_1\ s_0]$ is equal to the sum sequence $[(a_{N-2} + b_{N-2}) \ldots (a_1+b_1)(a_0+b_0)]$ and $c = [c_{N-1} \ldots c_1]$ is equal to the carry sequence associated with the sum sequence s.

17. A method for performing signal processing that requires multiplication of a first signal representing a binary number $a = [a_{N-1} \ldots a_1\ a_0]$ and a second signal representing a second binary number $b = [b_{N-1} \ldots b_1\ b_0]$, the method comprising:

receiving the first signal;

receiving the second signal;

forming a triangle array from the signal and the second signal, the triangle array including lines $k = 0$ to N-1; and

adding lines $k = 0$ to N-1.

18. The method according to claim 17, wherein forming the triangle array includes:

producing line $k = 0$ of the triangle array such that line $k = 0$ is equal to $[0\ (a_0 * b_0)]$;

producing lines $k = 1$ to N-1 of the triangle array such that lines $k = 1$ to N-1 are equal to $[p_1\ p0\ d_{k-1} \ldots d_1\ d_0]$, wherein the peak bits $[p_1\ p_0]$ for each line k are determined by:

$[p_1\ p0] = [0\ 0]$ if $a_k * b_k \neq 1$,

$[p1\ p0] = [1\ 0]$ if $[a_k * b_k = 1$ AND $c_k = 1]$, and

$[p1\ p0] = [0\ 1]$ if $[a_k * b_k = 1$ AND $c_k = 0]$,

wherein $[d_{k-1} \ldots d_1\ d_0]$ for each line k are determined by:

$[d_{k-1} \ldots d_1\ d_0] = [0_{k-1} \ldots 0_0]$ if $[a_k\ b_k] = [0\ 0]$,

$[d_{k-1} \ldots d_1\ d_0] = [a_{k-1} \ldots a_1\ a_0]$ if $[a_k\ b_k] = [0\ 1]$,

$[d_{k-1} \ldots d_1\ d_0] = [b_{k-1} \ldots b_1\ b_0]$ if $[a_k\ b_k] = [1\ 0]$, and

$[d_{k-1} \ldots d_1\ d_0] = [s_{k-1} \ldots s_1\ s_0]$ if $[a_k\ b_k] = [1\ 1]$,

and wherein $s = [s_{N-2} \ldots s_1\ s_0]$ is equal to the sum sequence $[(a_{N-2} + b_{k-2}) \ldots (a_1+b_1)\ (a_0+b_0)]$ and $c = [c_{N-1} \ldots c_1\ c_0]$ is equal to the carry sequence associated with the sum sequence s.